

WEST Search History

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DATE: Friday, April 08, 2005

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|--------------------------|--------------------------------------|---|----------------------------|
| | <i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i> | | |
| <input type="checkbox"/> | L83 | (cpu or processor) with L82 | 5 |
| <input type="checkbox"/> | L82 | L14 with (fpga or pld) | 70 |
| <input type="checkbox"/> | L81 | cpu with L79 | 12 |
| <input type="checkbox"/> | L80 | processor with L79 | 33 |
| <input type="checkbox"/> | L79 | L14 with (programmable gate\$1 or programmable logic) | 210 |
| <input type="checkbox"/> | L78 | L77 not (L65 or L63 or L61 or L60 or L58 or L70 or L75) | 270 |
| <input type="checkbox"/> | L77 | processor with L74 | 324 |
| <input type="checkbox"/> | L76 | L75 not (L65 or L63 or L61 or L60 or L58 or L70) | 6 |
| <input type="checkbox"/> | L75 | cpu same L74 | 43 |
| <input type="checkbox"/> | L74 | L15 with (programmable gate\$1 or programmable logic) | 1486 |
| <input type="checkbox"/> | L73 | L70 not (L65 or L63 or L61 or L60 or L58) | 18 |
| <input type="checkbox"/> | L72 | L70 not L58 | 18 |
| <input type="checkbox"/> | L71 | L70 not L60 | 20 |
| <input type="checkbox"/> | L70 | cpu same L69 | 26 |
| <input type="checkbox"/> | L69 | L15 with (fpga or pld) | 718 |
| <input type="checkbox"/> | L68 | L15 same (fpga or pld) | 1488 |
| | <i>DB=USPT,USOC; PLUR=NO; OP=ADJ</i> | | |
| <input type="checkbox"/> | L67 | L66 not (L65 or L63 or L61 or L60 or L58) | 44 |
| <input type="checkbox"/> | L66 | processor with L59 | 94 |
| <input type="checkbox"/> | L65 | processor with L62 | 50 |
| <input type="checkbox"/> | L64 | processor same L62 | 86 |
| <input type="checkbox"/> | L63 | core same L62 | 17 |
| <input type="checkbox"/> | L62 | L15 with (fpga or pld) | 168 |
| <input type="checkbox"/> | L61 | L60 not L58 | 17 |
| <input type="checkbox"/> | L60 | cpu same L59 | 23 |
| <input type="checkbox"/> | L59 | L15 with (programmable gate\$1 or programmable logic) | 460 |
| <input type="checkbox"/> | L58 | cpu same L57 | 18 |
| <input type="checkbox"/> | L57 | L15 same (fpga or pld) | 383 |
| <input type="checkbox"/> | L56 | cpu and L55 | 386 |
| <input type="checkbox"/> | L55 | L15 and (fpga or pld) | 1104 |
| <input type="checkbox"/> | L54 | logic integrated circuit\$1 and L22 | 0 |
| <input type="checkbox"/> | L53 | L22 and (programmable gate\$1 or programmable logic) | 0 |

| | | | |
|--|-----|---|-------|
| <input type="checkbox"/> | L52 | L22 and (fpga or pld) | 0 |
| <input type="checkbox"/> | L51 | enabl\$3 and (L2 or L6) | 2 |
| <input type="checkbox"/> | L50 | enabl\$3 and L49 | 1 |
| <input type="checkbox"/> | L49 | (L2 or L6) and programmable | 1 |
| <input type="checkbox"/> | L48 | (L2 or L6) and logic | 2 |
| <input type="checkbox"/> | L47 | L2 or L6 and logic | 2 |
| <input type="checkbox"/> | L46 | cpu with L44 | 4 |
| <input type="checkbox"/> | L45 | reprogram\$4 with L44 | 4 |
| <input type="checkbox"/> | L44 | fpga with (simulat\$3 or emulat\$3) | 312 |
| <i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ</i> | | | |
| <input type="checkbox"/> | L43 | reprogram\$4 with L42 | 0 |
| <input type="checkbox"/> | L42 | fpga with (simulat\$3 or emulat\$3) | 86 |
| <input type="checkbox"/> | L41 | fpga simulator | 0 |
| <i>DB=USPT; PLUR=NO; OP=ADJ</i> | | | |
| <input type="checkbox"/> | L40 | US-6260172-B1.did. | 1 |
| <input type="checkbox"/> | L39 | US-6089460-A.did. | 1 |
| <input type="checkbox"/> | L38 | US-6260172-B1.did. | 1 |
| <i>DB=PGPB; PLUR=NO; OP=ADJ</i> | | | |
| <input type="checkbox"/> | L37 | US-20010011214-A1.did. | 1 |
| <input type="checkbox"/> | L36 | US-20010011214-A1.did. | 1 |
| <i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ</i> | | | |
| <input type="checkbox"/> | L35 | cpu and L34 | 12 |
| <input type="checkbox"/> | L34 | logic integrated circuit\$1 | 925 |
| <i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i> | | | |
| <input type="checkbox"/> | L33 | 5968161.uref. | 6 |
| <input type="checkbox"/> | L32 | altera.as. and L31 | 1 |
| <input type="checkbox"/> | L31 | fpga same cpu | 1275 |
| <input type="checkbox"/> | L30 | altera.as. and cpu | 197 |
| <i>DB=USPT; PLUR=NO; OP=ADJ</i> | | | |
| <input type="checkbox"/> | L29 | cpu and L27 | 40 |
| <input type="checkbox"/> | L28 | cpu core\$1 and L27 | 1 |
| <input type="checkbox"/> | L27 | L26 and L15 | 129 |
| <input type="checkbox"/> | L26 | L12.ti,ab,clm. | 1510 |
| <input type="checkbox"/> | L25 | 5933642.pn. | 1 |
| <i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ</i> | | | |
| <input type="checkbox"/> | L24 | 5933642.pn. | 1 |
| <input type="checkbox"/> | L23 | L20 and L22 | 2 |
| <input type="checkbox"/> | L22 | firmware or nanoinstruction\$1 or nano-instruction\$1 or nanocode or nano-code or nanoprogram or nano-program or L21 | 16037 |
| <input type="checkbox"/> | L21 | microinstruction\$1 or micro-instruction\$1 or microcode or micro-code or micro-operation\$1 or microoperation\$1 or micro-op\$1 or microop\$1 or micro-program\$1 or microprogram\$1 | 11247 |

| | | | |
|--------------------------|-----|--|-------|
| <input type="checkbox"/> | L20 | cpu and L19 | 222 |
| <input type="checkbox"/> | L19 | field programmable gate array\$1 or fpga\$1 <i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i> | 3520 |
| <input type="checkbox"/> | L18 | cpu core\$1 and L17 | 12 |
| <input type="checkbox"/> | L17 | L12 same L15 | 1753 |
| <input type="checkbox"/> | L16 | L13 and L15 <i>DB=USPT,PGPB; PLUR=NO; OP=ADJ</i> | 98 |
| <input type="checkbox"/> | L15 | firmware or nanoinstruction\$1 or nano-instruction\$1 or nanocode or nano-code or nanoprogram or nano-program or L14 | 58062 |
| <input type="checkbox"/> | L14 | microinstruction\$1 or micro-instruction\$1 or microcode or micro-code or micro-operation\$1 or microoperation\$1 or micro-op\$1 or microop\$1 or micro- program\$1 or microprogram\$1 <i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i> | 14972 |
| <input type="checkbox"/> | L13 | cpu core\$1 and L12 | 150 |
| <input type="checkbox"/> | L12 | field programmable gate array\$1 or fpga\$1 | 18399 |
| <input type="checkbox"/> | L11 | L9 and core | 3138 |
| <input type="checkbox"/> | L10 | (L2 or L6) and L9 | 0 |
| <input type="checkbox"/> | L9 | field programmable gate array\$1 | 14226 |
| <input type="checkbox"/> | L8 | (L2 or L6) and fpga | 0 |
| <input type="checkbox"/> | L7 | (L2 or L6) and core | 0 |
| <input type="checkbox"/> | L6 | 5675777.pn. | 1 |
| <input type="checkbox"/> | L5 | glickman.in. and jeff.in. | 8 |
| <input type="checkbox"/> | L4 | glickman.in. and taraplex.as. | 0 |
| <input type="checkbox"/> | L3 | glickman.in. and teraplex.as. | 0 |
| <input type="checkbox"/> | L2 | 6389528.pn. | 1 |
| <input type="checkbox"/> | L1 | pappalardo.in. and tesi.in. | 7 |

END OF SEARCH HISTORY